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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/254,939	03/17/99	MIURA H	500.36904X00

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EXAMINER	
MAI,A	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 08/09/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/254,939	MIURA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *17 March 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fazan et al. (U.S. Patent No. 5,433,794).

Fazan teaches a method of fabricating a semiconductor device comprising the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor substrate (1);

(b) forming a trench (T) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate;

(c) oxidizing the trench portion (2A) formed in the semiconductor substrate;

(d) burying a buried insulating film (4) into the trench so oxidized;

(e) removing the buried insulating film (4) formed on said oxidation prevention film (3); and

(f) removing the oxidation prevention film formed on the circuit formation surface of the circuit substrate. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

3. Claim 7 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fazan '794.

Fazan teaches a semiconductor device of the type wherein a device isolation oxide film structure (4) formed on a circuit formation surface of a semiconductor substrate (1) is a trench isolation structure, characterized in that an angle θ of a trench, which constitutes the trench isolation structure with the circuit formation surface of the semiconductor substrate, in a depth-wise direction with respect to the side surface of the semiconductor substrate is within the range of $90° < \theta < 180°$.

4. Claim 8 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fazan '794.

Fazan teaches a semiconductor device of the type wherein a device isolation oxide film structure (4) formed on a circuit formation surface of a semiconductor substrate (1) is a trench isolation structure, characterized in that an angle θ of a trench, which constitutes the trench isolation structure with the circuit formation surface of the semiconductor substrate, in a depth-wise direction with respect to the side surface of the semiconductor substrate is within the range of $90° < \theta < 180°$, and a silicon oxide (4) exists inside the trench.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fäzan 794 in view of Miyashita et al. (EP. Patent No. 459397).

Fazan teaches a method of fabricating a semiconductor device substantially as claimed including the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor substrate (1);

(c) forming a trench having (T) a predetermined depth to the shallow trenches having a radius of curvature so formed;

(d) oxidizing the trench portions (2A) formed in the semiconductor substrate;

(e) burying a buried insulating film (4) into the trenches so oxidized;

(f) removing the buried insulating film formed on the oxidation prevention film (3); and

(g) removing the oxidation prevention film (3) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

Thus, Fazan is shown to teach all of the features of the claim with the exception of forming a shallow trenches having a radius of curvature at corners in a desired position of the circuit formation surface of the semiconductor substrate.

However, Miyashita '397 teaches forming shallow trenches (26) having a radius of curvature (27) at corners in a desired position of the circuit formation surface of the semiconductor substrate prior to forming the isolation trench (28) to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET. (See Figs. 2A-C, col. 2, l. 50-col. 3, l. 12).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the taper portion (27) at the corner of trench (T) of Fazan '794 as taught by Miyashita '397 to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET.

With respect to claim 3, the process for forming the shallow trench (26) of Miyashita '397 is carry out by isotropic etching and the step for forming the trench (28) is carry out by anisotropic etching.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan '794 in view of Perera (U.S. Patent No. 5,786,263).

Fazan teaches a method of fabricating a semiconductor device similar as claimed including the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor substrate (1);

(b) forming trenches (T) having a predetermined depth at desired positions of the circuit formation surface of the semiconductor substrate;

(c) oxidizing the trench portions (2A) formed in the semiconductor substrate;

(d) burying a buried insulating film (4) into the trenches so oxidized;

(e) removing the buried insulating film formed on the oxidation prevention film; and

(g) removing the oxidation prevention film (3) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

Thus, Fazan is shown to teach all of the features of the claim with the exception of oxidizing the semiconductor substrate (1) after the buried insulating film (4) formed on the oxidation prevention film is removed.

However, Perera teaches oxidizing the semiconductor substrate (12) after the buried insulating film (34) formed on the oxidation prevention film is removed. (See col. 4, ll. 9-21).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to oxidizing the semiconductor substrate (1) of Fazan after the buried insulating film (4) formed on the oxidation prevention film is removed to densify the buried insulating film.

7. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan '794 in view of Miyashita '397 and Perera '263.

Fazan teaches a method of fabricating a semiconductor device as claimed including the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor (1);

(c) forming trenches (T) having a predetermined depth in the semiconductor substrate;

(d) oxidizing the trench portions (2A) formed in the semiconductor substrate;

(e) burying a buried insulation film (4) into the trenches so oxidized;

(f) removing the buried insulating film formed on the oxidation prevention film (3); and

(h) removing the oxidation prevention film (3) formed on the circuit formation surface of the semiconductor substrate. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

Thus, Fazan is shown to teach all of the features of the claim with the exception of forming a shallow trench having a radius of curvature at corners prior to forming the trench (T) and oxidizing the semiconductor substrate (1) after the buried insulating film (4) formed on the oxidation prevention film (3) is removed.

However, Miyashita '397 teaches forming shallow trenches (26) having a radius of curvature (27) at corners in a desired position of the circuit formation surface of the semiconductor substrate prior to forming the isolation trench (28) to avoid the

concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET. (See Figs. 2A-C, col. 2, l. 50-col. 3, l. 12).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the taper portion (27) at the corner of trench (T) of Fazan '794 as taught by Miyashita '397 to avoid the concentration of electric field at the corner of the trench thereby preventing lowering the threshold voltage of the MOSFET.

Further, Perera teaches oxidizing the semiconductor substrate (12) after the buried insulating film (34) formed on the oxidation prevention film is removed. (See col. 4, ll. 9-21).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to oxidizing the semiconductor substrate (1) of Fazan after the buried insulating film (4) formed on the oxidation prevention film is removed to densify the buried insulating film.

With respect to claim 6, the process for forming the shallow trench (26) of Miyashita '397 is carry out by isotropic etching and the step for forming the trench (28) is carry out by anisotropic etching.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan '794 in view of Perera '263.

Fazan teaches a method of fabricating a semiconductor device similar as claimed including the steps of:

(a) forming an oxidation prevention film (3) on a circuit formation surface of a semiconductor substrate (1);

(b) forming trenches regions (T) in the substrate from the circuit formation surface thereof;

(c) performing a first oxidation to form an oxide film (2A) on the trench regions formed in step (b); and

(d) forming an insulating film (4) inside the oxidized trench regions so as to completely fill them. (See Figs. 3-6, col. 2, l. 25-col. 3, l. 33).

Thus, Fazan is shown to teach all of the features of the claim with the exception of performing a second oxidation to selectively oxidize the opening side of the completely filled trench regions in the substrate.

However, Perera teaches performing a second oxidation of the semiconductor substrate (12). (See col. 4, ll. 9-21).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to perform a second oxidation of the semiconductor substrate (1) of Fazan the trench is completely filled to densify the insulating film (4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Anh D. Mai
August 1, 2000

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